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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,708	02/06/2004	Mauricio Huerta Alva	200208228-1	8317

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EXAMINER	
KRAVETS, LEONID	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,708	ALVA ET AL.	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

1. Acknowledgment is made of the information disclosure statement received 6 February 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 14, 17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Desikan.

4. As per claim 14, Desikan discloses a method for reading data or instructions from a memory device that comprises a magneto-resistive random access memory (MRAM) coupled to a cache comprising:

receiving a request from a controller to read data from the MRAM (Desikan, Basic MRAM System Architecture);

determining if the requested data is located in the cache (Desikan, Basic MRAM System Architecture);

passing the data from the MRAM to the cache if the data is not located in the cache (Desikan, Basic MRAM System Architecture); and

passing the data to the controller from the cache (Desikan, Basic MRAM System Architecture).

5. As per claim 17, Desikan discloses a method for writing data to a memory device that comprises magneto-resistive random access memory (MRAM) coupled to a cache comprising:

receiving a request from a controller to write data to the MRAM;

determining if a memory block where the data is to be stored is located in the cache;

passing the memory block from the MRAM to the cache if the memory block is not located in the cache;

passing the data from the controller to the cache; and

passing the data from the cache to the MRAM.

[Desikan, Basic MRAM System Architecture]

6. As per claim 20, Desikan discloses a portable electronic device comprising:

a processor (Fig 3); and

a semiconductor memory device comprising:

a magneto-resistive random access memory (MRAM) (Fig 3);

a cache comprising a volatile memory (Fig 3, SRAM Cache); and

a control and address decoder configured to control the passing of data between the MRAM and the cache and between the cache and the processor (Fig 3, Bank Controller and Decoders).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-2, 4-6, 9-13, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desikan and further in view of Microsoft Computer Dictionary.

10. As per claim 1, Desikan discloses a memory device comprising:

a magneto-resistive random access memory (MRAM) (Fig 3);

a cache comprising a volatile memory (Fig 3); and

[Desikan discloses a decoder and that the MRAM is accessed using physical addresses (Page 6, Page Placement Policy)]. Desikan does not disclose a decoder configured to translate referenced addresses to physical addresses to access data and pass the data between the MRAM and the cache and between the cache and a controller.

The Microsoft Computer Dictionary discloses such a decoder configured to translate referenced addresses to physical addresses to access data and pass the data between the MRAM and the cache and between the cache and a controller (Memory Management Unit).

As per claim 2, Desikan and Microsoft disclose the memory device of claim 1, wherein the decoder translates referenced addresses from the controller to physical addresses in the MRAM and the cache (Microsoft, Memory Management Unit; Desikan, Fig 3).

As per claim 4, Desikan and Microsoft disclose the memory device of claim 1, wherein the cache comprises static random access memory (Desikan, Figure 3).

As per claim 5, Desikan and Microsoft disclose the memory device of claim 1, wherein the cache comprises dynamic random access memory [DRAM is a type of RAM, it would be obvious to substitute DRAM for SRAM since DRAM provides larger sizes].

As per claim 6, Desikan and Microsoft disclose the memory device of claim 1, wherein the cache, the MRAM, and the decoder are fabricated on a single semiconductor substrate (Desikan, Page 8, Baseline MRAM System).

As per claim 9, Desikan and Microsoft disclose a memory device comprising:

a magneto-resistive random access memory (MRAM) (fig 3, MRAM bank));

a volatile memory (Fig 3, SAM Cache); and

a virtual memory controller configured to pass data between the MRAM, the volatile memory, and a host (Fig 3). [Microsoft further discloses a memory management unit used to convert virtual addresses to physical addresses].

As per claim 10, Desikan and Microsoft disclose the memory device of claim 9, wherein the controller passes data between the volatile memory and the host based upon requests from the host (Fig 3, Bank Controller).

As per claim 11, Desikan and Microsoft disclose the memory device of claim 9, wherein the volatile memory comprises a static random access memory (Fig 3, SRAM Cache).

As per claim 12, Desikan and Microsoft disclose the memory device of claim 9, wherein the volatile memory comprises a dynamic random access memory [DRAM is a

type of RAM, it would be obvious to substitute DRAM for SRAM since DRAM provides larger sizes].

As per claim 13, Desikan and Microsoft disclose the memory device of claim 9, wherein a portion of the MRAM comprises a page file (Desikan, Page Placement Policy).

As per claim 16, Desikan discloses the method of claim 14, wherein the request comprises reference addresses, the method further comprising:

Desikan does not disclose the method further comprising translating the reference addresses to physical addresses.

Microsoft discloses such a method further for translating the reference addresses to physical addresses (Memory Management Unit).

As per claim 19, Desikan discloses the method of claim 17, wherein the request comprises reference addresses, the method further comprising:

Desikan does not disclose the method further comprising translating the reference addresses to physical addresses.

Microsoft discloses such a method further for translating the reference addresses to physical addresses (Memory Management Unit).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory management unit of Microsoft into the system of Desikan, since Desikan and Microsoft form the same field of endeavor, namely memory architecture and this would allow for translation of addresses from the virtual domain of the processor to the physical domain of memory.

11. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desikan and Microsoft as applied to claims 1 and 14 above, and further in view of Hilton (US Pub No 2004/0181733)

As per claim 3, Desikan and Microsoft disclose the memory device of claim 1.

They do not disclose an error detection and correction circuit electrically coupled to the cache and the MRAM, the error detection and correction circuit configured for error correction encoding and decoding of the data.

Hilton discloses such an error detection and correction circuit electrically coupled to the cache and the MRAM, the error detection and correction circuit configured for error correction encoding and decoding of the data (Paragraph 21, Fig 2).

As per claim 15, Desikan and Microsoft disclose the method of claim 14.

They do not disclose error correction decoding the data from the MRAM.

Hilton discloses error correction decoding the data from the MRAM (Paragraph 21, Fig 2)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the ECC circuit of Hilton into the system of Desikan and Microsoft, since Desikan, Microsoft and Hilton form the same field of endeavor, namely memory architecture and this would allow for correction of errors in memory transmission (Paragraph 19)

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Desikan and Microsoft as applied to claim 17 above, and further in view of Hilton.

As per claim 18, Desikan discloses the method of claim 17.

He does not disclose error correction encoding the data from the cache.

Hilton discloses error correction encoding the data from the cache (Paragraph 21, Fig 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the ECC circuit of Hilton into the system of Desikan, since Desikan and Hilton form the same field of endeavor, namely memory architecture and this would allow for correction of errors in memory transmission (Paragraph 19).

13. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desikan and Microsoft as applied to claim 1 above, and further in view of Vaidya (US Pub No 2004/0225843).

As per claim 7, Desikan and Microsoft disclose the memory device of claim 1, Desikan and Microsoft do not disclose the memory device wherein the cache comprises one of a unified cache and a segmented cache.

Vaidya discloses a memory device wherein the cache comprises one of a unified cache and a segmented cache (Fig 1, Ref 20, 22; Paragraph 15)

As per claim 8, Desikan, Microsoft and Vaidya disclose the memory device of claim 7, wherein the segmented cache comprises a data segment and an instructions segment (Fig 1, Ref 20, 22; Paragraph 15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the segmented cache of Vaidya into the system of Desikan and Microsoft, since Desikan, Microsoft and Vaidya form the same field of endeavor, namely CPU caches and this would allow for that an instruction may be read and a load or store operation performed simultaneously (Vaidya, Paragraph 1).

14. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desikan as applied to claim 20 above, and further in view of Butner.

As per claim 21, Desikan discloses the portable electronic device of claim 20, Desikan does not disclose that the portable electronic device comprises a display. Butner discloses that the portable electronic device comprises a display [...devices such as PDAs and cell phones will require the dense, fast, relatively inexpensive nonvolatile memory that MRAM can provide]

As per claim 22, Desikan and Butner disclose the portable electronic device of claim 20, wherein the portable electronic device is one of a personal digital assistant, a cellular telephone, a digital music player, a personal organizer, and a digital camera [Butner, ...devices such as PDAs and cell phones will require the dense, fast, relatively inexpensive nonvolatile memory that MRAM can provide].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the portable device of Butner into the system of Desikan, since Desikan and Butner form the same field of endeavor, namely MRAM storage systems and this would allow for dense, fast, relatively inexpensive nonvolatile memory that such devices require (Butner, Setting the standard).

Conclusion

15. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 16, 2006

Leonid Kravets
Patent Examiner
Art Unit 2189

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER